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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/827,360	04/20/2004	Richard Carl Phelps	0120-030	2608

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EXAMINER	
CLEARY, THOMAS J	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 08/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/827,360	PHELPS ET AL.	
	Examiner	Art Unit	
	Thomas J. Cleary	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 2, 3, 5, and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Japanese Patent Number JP 08147163 to Takemoto ("Takemoto").

3. In reference to Claim 1, Takemoto discloses an apparatus for use in a computer system comprising: a pipeline bus architecture, in which data traverses the bus architecture over a plurality of system clock cycles (See Figure 1); a plurality of modules connected to the bus architecture (See Figure 1 Numbers 15, 17, and 19); wherein the bus architecture comprises: a plurality of bus connection units (See Figure 1 Numbers 16, 18, and 20); and a plurality of bus portions arranged in series, each bus portion, except the last in the series, being connected to the next portion in the series by way of a bus connection unit (See Figure 1), wherein each of the modules is connected to the bus architecture by way of a respective one of the bus connection units (See Figure 1 Numbers 16, 18, and 20); and each of the bus connection units including multiplexer

circuitry for selectively connecting a module to the bus architecture (See Figure 1 Numbers 16, 18, and 20).

4. In reference to Claim 2, Takemoto discloses the limitations as applied to Claim 1 above. Takemoto further discloses that each bus connection unit includes output circuitry connected to the bus portions to which the unit is connected, the output circuitry being tailored to optimize the signal characteristics for the length of the bus portions concerned (See 'Purpose' in English Language Abstract).

5. In reference to Claim 3, Takemoto discloses the limitations as applied to Claim 1 above. Takemoto further discloses that the bus portions are all equal in length (See Figure 1).

6. In reference to Claim 5, Takemoto discloses the limitations as applied to Claim 1 above. Takemoto further discloses that a central arbitration unit arbitrates between the modules in order to grant access to the bus architecture (See Figure 1 Number 21).

7. In reference to Claim 12, Takemoto discloses the limitations as applied to Claim 1 above. Takemoto further discloses a computer system comprising the apparatus (See Figure 1).

8. Claims 1, 2, 3, 5, and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent Number 5,325,495 to McLellan ("McLellan").

9. In reference to Claim 1, McLellan discloses an apparatus for use in a computer system comprising: a pipeline bus architecture, in which data traverses the bus architecture over a plurality of system clock cycles (See Figure 1); a plurality of modules connected to the bus architecture (See Figure 1 Numbers 16 and 16'); wherein the bus architecture comprises: a plurality of bus connection units (See Figure 1 Numbers 18 and 18'); and a plurality of bus portions arranged in series, each bus portion, except the last in the series, being connected to the next portion in the series by way of a bus connection unit (See Figure 1 'Q-Stage' and 'Pipeline Stage 4'), wherein each of the modules is connected to the bus architecture by way of a respective one of the bus connection units (See Figure 1 Numbers 18 and 18'); and each of the bus connection units including multiplexer circuitry for selectively connecting a module to the bus architecture (See Figure 1 Numbers 18 and 18').

10. In reference to Claim 2, McLellan discloses the limitations as applied to Claim 1 above. McLellan further discloses that each bus connection unit includes output circuitry connected to the bus portions to which the unit is connected, the output circuitry being tailored to optimize the signal characteristics for the length of the bus portions concerned (See Column 4 Lines 38-44).

11. In reference to Claim 3, McLellan discloses the limitations as applied to Claim 1 above. McLellan further discloses that the bus portions are all equal in length (See Figure 1).

12. In reference to Claim 5, McLellan discloses the limitations as applied to Claim 1 above. McLellan further discloses that a central arbitration unit arbitrates between the modules in order to grant access to the bus architecture (See Figure 1 Number 20).

13. In reference to Claim 12, McLellan discloses the limitations as applied to Claim 1 above. McLellan further discloses a computer system comprising the apparatus (See Figure 1).

14. Claims 1, 2, 3, 5, and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent Number 5,555,384 to Roberts et al. ("Roberts").

15. In reference to Claim 1, Roberts discloses an apparatus for use in a computer system comprising: a pipeline bus architecture, in which data traverses the bus architecture over a plurality of system clock cycles (See Figure 6); a plurality of modules connected to the bus architecture (See Figure 6 'Execution Unit(s) and Numbers 33 and 35); wherein the bus architecture comprises: a plurality of bus connection units (See Figure 6); and a plurality of bus portions arranged in series, each bus portion, except the last in the series, being connected to the next portion in the series by way of a bus

connection unit (See Figure 6), wherein each of the modules is connected to the bus architecture by way of a respective one of the bus connection units (See Figure 6 'Execution Unit(s) and Numbers 33 and 35); and each of the bus connection units including multiplexer circuitry for selectively connecting a module to the bus architecture (See Figure 6).

16. In reference to Claim 2, Roberts discloses the limitations as applied to Claim 1 above. Roberts further discloses that each bus connection unit includes output circuitry connected to the bus portions to which the unit is connected, the output circuitry being tailored to optimize the signal characteristics for the length of the bus portions concerned (See Column 5 Lines 42-49).

17. In reference to Claim 3, Roberts discloses the limitations as applied to Claim 1 above. Roberts further discloses that the bus portions are all equal in length (See Figure 6).

18. In reference to Claim 5, Roberts discloses the limitations as applied to Claim 1 above. Roberts further discloses that a central arbitration unit arbitrates between the modules in order to grant access to the bus architecture (See Figure 6 Number 50).

19. In reference to Claim 12, Roberts discloses the limitations as applied to Claim 1 above. Roberts further discloses a computer system comprising the apparatus (See Figure 6).

Claim Rejections - 35 USC § 103

20. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

21. Claims 4, 6, 7, and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takemoto as applied to Claims 1 and 5 above, and further in view of US Patent Number 5,627,976 to McFarland et al. ("McFarland").

22. In reference to Claim 4, Takemoto teaches the limitations as applied to Claim 1 above. Takemoto does not teach a primary bus and a secondary bus, the primary and secondary buses being interconnected by an interface. McFarland teaches a primary bus (See Figure 1 Number 20) and secondary bus (See Figure 1 Number 25) interconnected by an interface (See Figure 1 Number 45), a plurality of modules connected to the primary bus (See Figure 1 Numbers 32, 35, and 37), and a plurality of modules connected to the secondary bus (See Figure 1 Numbers 40 and 42).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the dual bus system of McFarland with the pipelined bus structure of Takemoto, resulting in the invention of Claim 4, because a dual bus system allows a very fast bus to interface with a much slower bus in a way that the high bandwidth of the former is maintained except when a device on the former and a device on the latter need to communicate (See Column 2 Lines 61-65 of McFarland) and because pipelines with bypass stages reduce power consumption (See 'Purpose' in English Language Abstract of Takemoto).

23. In reference to Claim 6, Takemoto teaches the limitations as applied to Claim 5 above. Takemoto does not teach a primary bus and a secondary bus, the primary and secondary buses being interconnected by an interface. McFarland teaches a primary bus (See Figure 1 Number 20) and secondary bus (See Figure 1 Number 25) interconnected by an interface (See Figure 1 Number 45), a plurality of modules connected to the primary bus (See Figure 1 Numbers 32, 35, and 37), and a plurality of modules connected to the secondary bus (See Figure 1 Numbers 40 and 42).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the dual bus system of McFarland with the pipelined bus structure of Takemoto, resulting in the invention of Claim 6, because a dual bus system allows a very fast bus to interface with a much slower bus in a way that the high bandwidth of the former is maintained except when a device on the former and a device on the latter need to communicate (See Column 2 Lines 61-65 of McFarland) and

because pipelines with bypass stages reduce power consumption (See 'Purpose' in English Language Abstract of Takemoto).

24. In reference to Claim 7, Takemoto and McFarland teach the limitations as applied to Claim 4 above. McFarland further teaches that the first plurality of modules are latency tolerant and the second plurality of modules are latency intolerant (See Figure 1, Column 2 Line 61 – Column 3 Line 12 and Column 5 Lines 21-32).

25. In reference to Claim 8, Takemoto and McFarland teach the limitations as applied to Claim 4 above. McFarland further teaches that the primary bus is one pipeline stage in length (See Figure 1).

26. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takemoto as applied to Claim 1 above, and further in view of US Patent Number 5,128,926 to Perlman et al. ("Perlman").

27. In reference to Claim 9, Takemoto teaches the limitations as applied to Claim 1 above. Takemoto does not teach that transactions involving data in excess of a predetermined size are split into a plurality of data packets of fixed size, said packets being independently arbitrated. Perlman teaches splitting a large packet into pieces which are smaller than the maximum packet size and transmitting the smaller packets separately (See Column 2 Lines 55-58).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Takemoto with the packet splitting of Perlman, resulting in the invention of Claim 9, in order to relieve the computation burden by reducing the probability of errors in transmission (See Column 2 Line 64 – Column 3 Line 14 of Perlman).

28. Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takemoto as applied to Claim 1 above, and further in view of US Patent Number 5,925,118 to Revilla et al. ("Revilla").

29. In reference to Claim 10 Takemoto teaches the limitations as applied to Claim 1 above. Takemoto does not teach separate read, write, and transaction buses. Revilla teaches the use of separate read (See Figure 1 Number 34), write (See Figure 1 Number 32), and transaction buses (See Figure 1 Number 36).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Takemoto with the split bus system of Revilla, resulting in the invention of Claim 10, in order to provide a high throughput of data between functions (See Column 2 Lines 17-31 of Revilla).

30. In reference to Claim 11 Takemoto teaches the limitations as applied to Claim 1 above. Takemoto does not teach that the bus architecture has a width sufficient to permit read and write request transactions to alternate in successive system clock

cycles. Revilla teaches the use of separate read (See Figure 1 Number 34), write (See Figure 1 Number 32), and transaction buses (See Figure 1 Number 36) which have a width sufficient to permit read and write request transactions to alternate in successive system clock cycles (See Column 3 Lines 12-26).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Takemoto with the split bus system of Revilla, resulting in the invention of Claim 11, in order to provide a high throughput of data between functions (See Column 2 Lines 17-31 of Revilla).

Response to Arguments

31. Applicant's arguments filed 12 June 2006 have been fully considered but they are not persuasive.

32. Applicant has argued that the processors of Takemoto are not connected to the bus stages through the multiplexers (See Page 5 Paragraph 4). In response, the Examiner notes, that, as shown in the above rejections, it is the registers (See Figure 1 Numbers 15, 17, and 19), and not the processors (See Figure 1 numbers 13 and 14), of Takemoto that have been equated to the claimed modules. Registers 15, 17, and 19 are each connected to the bus structure through multiplexers 16, 18, and 20, respectively. When the multiplexer is set to transmit data from the register, the register is connected to the bus architecture. Conversely, when the multiplexer is set to bypass

the register, the register is no longer connected to the bus architecture. Thus, the multiplexer selectively connects the registers to the bus architecture.

33. Applicant has argued that the multiplexers of McLellan are not used for selectively connecting a module to the bus architecture, the modules are permanently connected to the bus architecture, and that each bus portion is not connected to the next portion by way of a bus connection unit (See Page 6 Paragraph 5). In response, the Examiner notes that McLellan discloses two bus portions (See Figure 1 'Q-STAGE' and 'PIPELINE STAGE-4'), which is a plurality of bus portions. The registers of the Q-STAGE (See Figure 1 Numbers 16 and 16') are equivalent to the claimed plurality of modules. The Q-STAGE bus portion is connected to the PIPELINE STAGE-4 bus portion by way of a bus connection unit comprising multiplexer circuitry (See Figure 1 Numbers 18 and 18'). When the multiplexer is set to transmit data from a Q register, the register is connected to the bus architecture. Conversely, when the multiplexer is set to bypass the Q register, the register is no longer connected to the bus architecture. Thus, the multiplexer selectively connects the registers to the bus architecture.

34. Applicant has argued that Roberts does not disclose each of the bus connecting units including multiplexer circuitry for selectively connecting a module to the bus architecture (See Page 7 Paragraph 3). In response, the Examiner notes that, as shown in the above rejections, it is the Execution Unit(s) and registers 33 and 35, and not registers 33, 35, and 37, of Roberts that have been equated to the claimed modules.

The Execution Unit(s) and registers 33 and 35 (hereinafter "modules") are each connected to the bus structure through a multiplexer (See Figure 6). When the multiplexer is set to transmit data from the module, the module is connected to the bus architecture. Conversely, when the multiplexer is set to bypass the module, the module is no longer connected to the bus architecture. Thus, the multiplexer selectively connects the modules to the bus architecture.

35. Applicant has argued that the claimed modules are not "in-line" with the pipeline bus (See Page 8 Paragraph 2). In response, the Examiner notes that the features upon which applicant relies (i.e., modules that are not "in-line") are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Further, each of Takemoto, McLellan, and Roberts disclose modules which can be bypassed. If a module can be bypassed, it is not "in-line" with the bus.

Conclusion

36. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas J. Cleary whose telephone number is 571-272-3624. The examiner can normally be reached on Monday-Thursday (7-3), Alt. Fridays (7-2).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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